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Documentation - Arm Developer
Cortex-M3 Technical Reference Manual . Preface; Introduction; Functional Description; Programmers Model. About the programmers model; Modes of operation and execution; Instruction set summary; System address map; Write buffer; Exclusive monitor; Bit-banding; Processor core register summary; Exceptions; System Control; Memory Protection Unit ...

Cortex-M3 Technical Reference Manual | Programmers Model ...
This document provides the information required to use the ARM Cortex-M3 core in EFM32 microcontrollers. Further details on the specific implementations within the EFM32 devices can be found in the reference manual and datasheet for the specific device. This document does not provide information on debug components, features, or operation.

EFM32 Cortex-M3 Reference Manual - Silicon Labs
Cortex-M3 Technical Reference Manual: Revision r2p0; Home > Data Watchpoint and Trace Unit > DWT Programmers Model: 8.3. DWT Programmers Model. Table 8.1 lists the DWT registers. Depending on the implementation of your processor, some of these registers might not be present.

Cortex-M3 Technical Reference Manual: 8.3. DWT Programmers ...
• ARMv7-M Architecture Reference Manual (ARM DDI 0403) • ARM Cortex-M4 Integration and Implementation Manual (ARM DDI 0239) • ARM ETM-M4 Technical Reference Manual (ARM DDI 0440) • ARM AMBA® 3 AHB-Lite Protocol (v1.0) (ARM IHI 0033) • ARM AMBA™ 3 APB Protocol Specification (ARM IHI 0024)

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Technical Reference Manual Literature Number: SWCU1171 February 2015–Revised June 2020. 2 SWCU1171–February 2015–Revised June 2020 ... 3.2.8 Cortex-M3 Memory Map ... 10.8.1 Conventions Used in This Manual ...

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Title: Cortex-M3 Technical Reference Manual Author: ARM Limited Subject: ARM Cortex-M3 Technical Reference Manual (TRM). This guide contains documentation for the Cortex-M3 processor, describing the programmer's model, instructions, registers, memory map, cache and debug support.

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1.3 About the STM32 Cortex®-M3 processor and core peripherals The Cortex-M3 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and

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to the STM32F100xx Flash programming manual (PM0063). For information on the ARM® Cortex®-M3 core, refer to the Cortex®-M3 Technical Reference Manual. Related documents Available from www.arm.com: • Cortex®-M3 Technical Reference Manual Available from www.st.com: • STM32F100xx datasheets • STM32F100xx Flash programming manual www.st.com

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Parameters Protocols Bluetooth 5.1 Features LE 1M PHY, LE 2M PHY, LE Coded PHY (long range) Flash (KB) 128 CPU core Arm Cortex-M3 Type Wireless MCU RAM (KB) 20 GPIO 10, 14, 15, 31 Peripherals 1 UART, 12-bit ADC 8-channel, 2 SPI, 4 timers, 8-bit DAC, I2C, I2S, Sensor controller Security Cryptographic acceleration, Debug security, Device identity, Software IP protection Sensitivity (best) (dBm ...

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